WHAT IS CLAIMED IS:

1. A method of fabricating polycrystalline silicon thin film transistor, the method comprising the steps of:

depositing a buffer layer on a substrate;

depositing an amorphous silicon layer on the buffer layer with a predetermined thickness;

crystallizing the deposited amorphous silicon layer by using a laser to form a polycrystalline silicon layer;

etching the crystallized polycrystalline silicon layer to a predetermined thickness;

curing the etched polycrystalline silicon layer; and

patterning the cured polycrystalline silicon layer to form a semiconductor layer.

2. The method according to claim 1, wherein the amorphous silicon layer is deposited with a thickness of about 700 - 10000 Å.

3. The method according to claim 1, wherein the crystallizing uses an excimer laser.

4. The method according to claim 3, wherein an excimer laser crystalizing process uses one of an excimer laser process and a sequential lateral solidification process.

5. The method according to claim 1, wherein the crystallized polycrystalline silicon layer is etched to a thickness according to a channel resistance, and wherein the polycrystalline silicon layer has a thickness to achieve a desired on-current drive for the thin film transistor.

6. The method according to claim 1, wherein the crystallized polycrystalline silicon layer is etched according to a process margin for etching a subsequent contact hole to contact a source/drain electrode and wherein the etched polycrystalline silicon layer is thicker than a predetermined thickness.

7. The method according to claim 1, wherein the polycrystalline silicon layer is etched to a thickness of about 100 - 600 Å.

8. The method according to claim 1, wherein the crystallized polycrystalline silicon layer is etched to the predetermined thickness by using a chemical mechanical polishing process.

9. The method according to claim 1, wherein the crystallized polycrystalline silicon layer is etched to the predetermined thickness by using an etch-back process.

10. The method according to claim 1, wherein the etched polycrystalline silicon layer is cured at a temperature of about 400 – 500 °C.

11. The method according to claim 1, wherein the etched polycrystalline silicon layer is cured using a laser annealing process.

12. The method according to claim 1, wherein the etched polycrystalline silicon layer is cured using a rapid thermal annealing process.

13. The method according to claim 1, further comprising the steps of:

forming a first insulating film on the formed layers;

depositing a metal film on the first insulating film and forming a gate electrode by patterning the metal film;

forming a second insulating film on the layers on which the gate electrode is formed;

forming a first contact hole and a second contact hole to the semiconductor layer by etching the first and second insulating films on the semiconductor layer so that a portion of the semiconductor layer is exposed;

depositing a metal film on the second insulating film and patterning the metal film to form a source electrode and a drain electrode connected electrically to the semiconductor layer through the first contact hole and the second contact hole;

forming a passivation film on the formed source/drain electrode;

forming a third contact hole in the passivation film to the drain electrode; and

forming a pixel electrode connected electrically to the drain electrode through the third contact hole by depositing a transparent conductive film on the layers and patterning the transparent conductive film.

14. A method of fabricating a polycrystalline silicon thin film transistor, the method comprising the steps of:

depositing an amorphous silicon layer on a substrate at a predetermined thickness;

crystallizing the deposited amorphous silicon layer to form a polycrystalline silicon layer;

reducing the thickness of the crystallized polycrystalline silicon layer to a predetermined thickness; and

patterning the reduced polycrystalline silicon layer to form a semiconductor layer.

15. The method according to claim 14, wherein the amorphous silicon layer is deposited at a thickness of about 700 - 10000 Å.

16. The method according to claim 14, wherein crystallizing uses an excimer laser.

17. The method according to claim 16, an excimer laser crystalizing process uses one of an excimer laser process and a sequential lateral solidification process.

18. The method according to claim 14, wherein the crystallized polycrystalline silicon layer is reduced to a thickness according to a channel resistance, and wherein the polycrystalline silicon layer has a thickness to achieve a desired on-current drive for the thin film transistor.

19. The method according to claim 14, the crystallized polycrystalline silicon layer is reduced according to of a process margin for etching a subsequent contact hole to contact a source/drain electrode, and wherein the polycrystalline silicon layer is thicker than a predetermined thickness.

20. The method according to claim 14, the polycrystalline silicon layer is reduced

to a thickness of about 100 - 600 Å.

21. The method according to claim 14, wherein the crystallized polycrystalline silicon layer is reduced to a predetermined thickness by using a chemical mechanical polishing process.

22. The method according to claim 14, wherein the crystallized polycrystalline silicon layer is reduced to a predetermined thickness by using an etch-back process.

23. The method according to claim 14, further comprising the steps of:

forming a first insulating film on the formed layers;

depositing a metal film on the first insulating film and forming a gate electrode by patterning the metal film;

forming a second insulating film on the layers on which the gate electrode is formed;

forming a first contact hole and a second contact hole to the semiconductor layer by etching the first and second insulating films on the semiconductor layer so that a portion of the semiconductor layer is exposed;

depositing a metal film on the second insulating film and patterning the metal film to form a source electrode and a drain electrode connected electrically to the semiconductor layer through the first contact hole and the second contact hole;

forming a passivation film on the formed source/drain electrode;

forming a third contact hole in the passivation film provided on the drain electrode; and

forming a pixel electrode connected electrically to the drain electrode through the third contact hole by depositing a transparent conductive film on the layers and patterning the transparent conductive film.